This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having an indented section;

a gate dielectric layer disposed on the indented section;

a gate electrode disposed on the gate dielectric layer, wherein a portion of the gate electrode is embedded in the semiconductor substrate and another portion of the gate electrode is above the semiconductor substrate;

first and second impurity diffusion layers disposed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them;

a third impurity diffusion layer disposed in a portion immediately below the gate electrode in the semiconductor substrate; and

a sidewall dielectric layer disposed on a side surface section of the gate electrode,

wherein the gate electrode has a width that gradually increases from a bottom thereof up to an upper surface thereof, ~~and~~

wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer; and

wherein a majority of the gate electrode and a majority of the sidewall dielectric layer are above the semiconductor substrate, and first and second impurity diffusion layers.

2. (Original) A semiconductor device according to claim 1, wherein a distance between the surface of the first and second impurity diffusion layers and the interface between the semiconductor substrate and the gate dielectric layer is between about 0.05 and 0.15 μm.

3. (Previously Amended) A semiconductor device according to claim 1, wherein a groove section is disposed at a specified location in the semiconductor substrate, and the gate electrode is disposed on a bottom surface of the groove section through the gate dielectric layer.

4. (Previously Amended) A semiconductor device according to claim 1, wherein the gate electrode is disposed from at least one alloy that includes at least two constituents selected from the following group:

polycrystalline silicon, tungsten, tantalum, copper and gold.

5. – 6. (Previously Cancelled)

7. (Previously Presented) A semiconductor device according to claim 1, wherein the first and second impurity diffusion layers include an extension region.

8. (Cancelled)

9. (Previously Amended) A semiconductor device according to claim 1, wherein a first metal silicide layer is disposed on the first and second impurity diffusion layers, and the gate electrode includes a second metal silicide layer on an upper surface thereof.

10. (Cancelled)

11. (Previously Amended) A semiconductor device according to claim 1, wherein surfaces of the first and second impurity diffusion layers are disposed at a position higher than a surface of an element isolation region.

12 – 20 (Cancelled)

21. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having an indented section;

a gate dielectric layer disposed on the indented section;

a gate electrode disposed on the gate dielectric layer, wherein a portion of the gate electrode is embedded in the semiconductor substrate and another portion of the gate electrode is above the semiconductor substrate;

first and second impurity diffusion layers disposed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them; and

a sidewall dielectric layer disposed on a side surface section of the gate electrode,

wherein the gate electrode has a width that gradually increases from a bottom thereof up to an upper surface thereof,

wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, and

wherein surfaces of the first and second impurity diffusion layers are disposed at a position higher than a surface of an element isolation region; and

wherein a majority of the gate electrode and a majority of the sidewall dielectric layer are above the semiconductor substrate, and first and second impurity diffusion layers.

22. (Previously Presented) A semiconductor device according to claim 21, wherein a distance between the surface of the first and second impurity diffusion layers and the interface between the semiconductor substrate and the gate dielectric layer is between about 0.05 and 0.15 μm.

23. (Previously Amended) A semiconductor device according to claim 21, wherein a groove section is disposed at a specified location in the semiconductor substrate, and the gate electrode is disposed on a bottom surface of the groove section through the gate dielectric layer.

24. (Previously Amended) A semiconductor device according to claim 21, wherein the gate electrode is disposed from at least one alloy that includes at least two constituents selected from the following group:

polycrystalline silicon, tungsten, tantalum, copper and gold.

25.-27. (Cancelled)

28. (Previously Presented) A semiconductor device according to claim 21, further comprising:

a third impurity diffusion layer immediately below the gate electrode in the semiconductor substrate, wherein the third impurity diffusion layer is of the opposite conductivity type as the semiconductor substrate, and wherein the first and second impurity diffusion layers include an extension region.

29. (Previously Amended) A semiconductor device according to claim 21, wherein a first metal silicide layer is disposed on the first and second impurity diffusion layers, and the gate electrode includes a second metal silicide layer on an upper surface thereof.

30. (Cancelled)

31. (Previously Amended) A semiconductor device according to claim 21, wherein the sidewall dielectric layer has an outer surface that is generally vertical with respect to the surface of the semiconductor substrate, and a film thickness that gradually reduces from a bottom thereof up to an upper surface thereof.

32. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having an indented section;

a gate dielectric layer disposed on the indented section;

a groove section disposed at a specified location in the semiconductor substrate;

first and second impurity layers disposed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them;

a gate electrode disposed on the gate substrate and another portion of the gate electrode is above the semiconductor substrate,

wherein the gate electrode has a width that gradually increases from a bottom thereof up to an upper surface thereof, and a width of the upper surface of the gate electrode substantially equals the width of the groove; and

wherein a majority of the gate electrode and a majority of a sidewall dielectric layer disposed on a side surface section of the gate electrode are above the semiconductor substrate and above the first and second impurity diffusion layers.

33. (Cancelled)

34. (Previously Amended) A semiconductor device according to claim 1, wherein a majority of the gate electrode is above the semiconductor substrate, and the first and second impurity diffusion layers.

35. (Previously Presented) A semiconductor device according to claim 1, wherein the third impurity diffusion layer is completely disposed between the first and second impurity diffusion layers.

36. (Previously Amended) A semiconductor device according to claim 7, wherein the extension regions are below the sidewall dielectric layer, and wherein an area below the gate dielectric layer is free of the extension regions.

37. (Cancelled).

38. (Previously amended) A semiconductor device according to claim 21, wherein a majority of the gate electrode is above the semiconductor substrate, and the first and second impurity diffusion layers.

39. (Previously Presented) A semiconductor device according to claim 28, wherein the third impurity diffusion layer is completely disposed between the first and second impurity diffusion layers.

40. (Previously Presented) A semiconductor device according to claim 28, wherein the extension regions of the first and second impurity diffusion layers are below the sidewall dielectric layer, and wherein an area below the gate dielectric layer is free of the extension regions.

41. (Cancelled)

42. (Previously Presented) A semiconductor device according to claim 32, wherein a third impurity diffusion layer is completely disposed between the first and second impurity diffusion layers.

43. (Previously Presented) A semiconductor device according to claim 32, further comprising:

extension regions in the first and second impurity diffusion layers, wherein the extension regions are below the sidewall dielectric layer, and wherein an area below the gate dielectric layer is free of the extension regions.

44. (Previously Presented) A semiconductor device according to claim 1, wherein the gate electrode has a width that continuously increases from a bottom thereof up to an upper surface thereof.

45. (Previously Presented) A semiconductor device according to claim 1, wherein the semiconductor substrate has a first surface and the indented section has a second surface below the first surface, and wherein the entire gate dielectric layer is disposed on the second surface.

46. (Previously Presented) A semiconductor device according to claim 45, wherein the sidewall dielectric layer and the gate dielectric layer are disposed in contact with the indented section.

47. (Previously Presented) A semiconductor device according to claim 45, wherein the sidewall dielectric layer has an outer surface that is substantially vertical with respect to the first surface of the semiconductor substrate .

48. (Previously Presented) A semiconductor device according to claim 47, wherein the sidewall dielectric layer surrounds the gate dielectric layer.

49. (Previously Presented) A semiconductor device according to claim 9, wherein at least a portion of the gate dielectric layer is above at least a portion of the sidewall dielectric layer, and wherein the sidewall dielectric layer is formed below the second metal silicide layer.

50. (Previously Presented) A semiconductor device according to claim 1, wherein a majority of the gate electrode is above the semiconductor substrate, the first impurity diffusion layer, and the second impurity diffusion layer.

51. (Previously Presented) A semiconductor device according to claim 21, wherein the gate electrode has a width that continuously increases from a bottom thereof up to an upper surface thereof.

52. (Previously Presented) A semiconductor device according to claim 21, wherein the semiconductor substrate has a first surface and the indented section has a second surface below the first surface, and wherein the entire gate dielectric layer is disposed on the second surface.

53. (Previously Presented) A semiconductor device according to claim 52, wherein the sidewall dielectric layer and the gate dielectric layer are disposed in contact with the indented section.

54. (Previously Presented) A semiconductor device according to claim 31, wherein the sidewall dielectric layer surrounds the gate dielectric layer.

55. (Previously Presented) A semiconductor device according to claim 29, wherein at least a portion of the gate dielectric layer is above at least a portion of the sidewall dielectric layer, and wherein the sidewall dielectric layer is formed below the second metal silicide layer.

56. (Previously Presented) A semiconductor device according to claim 32, wherein the gate electrode has a width that continuously increases from a bottom thereof up to an upper surface thereof.

57. (Previously Presented) A semiconductor device according to claim 32, wherein the semiconductor substrate has a first surface and the indented section has a second surface below the first surface, and wherein the entire gate dielectric layer is disposed on the second surface.

58. (Previously Presented) A semiconductor device according to claim 57, wherein the sidewall dielectric layer and the gate dielectric layer are disposed in contact with the indented section.

59. (Previously Presented) A semiconductor device according to claim 57, wherein the sidewall dielectric layer has an outer surface that is substantially vertical with respect to the first surface of the semiconductor substrate .

60. (Previously Presented) A semiconductor device according to claim 59, wherein the sidewall dielectric layer surrounds the gate dielectric layer and wherein at least a portion of the gate dielectric layer is above at least a portion of the sidewall dielectric layer.

61. (Previously Presented) A semiconductor device according to claim 32, wherein a first metal silicide layer is disposed on the first and second impurity diffusion layers, and

wherein the gate electrode includes a second metal silicide layer on an upper surface thereof and the sidewall dielectric layer is formed below the second metal silicide layer.

62. (Previously Presented) A semiconductor device according to claim 32, wherein surfaces of the first and second impurity diffusion layers are disposed at a position higher than a surface of an element isolation region.

63. (Previously Presented) A semiconductor device according to claim 32, wherein a majority of the gate electrode is above the semiconductor substrate, and the first and second impurity diffusion layers.